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Understanding The Transient Response Of A Switch-Mode Supply

Fast-Changing Load Currents And Extended Cabling Can Conspire To Jeopardize An Otherwise Sound Design.

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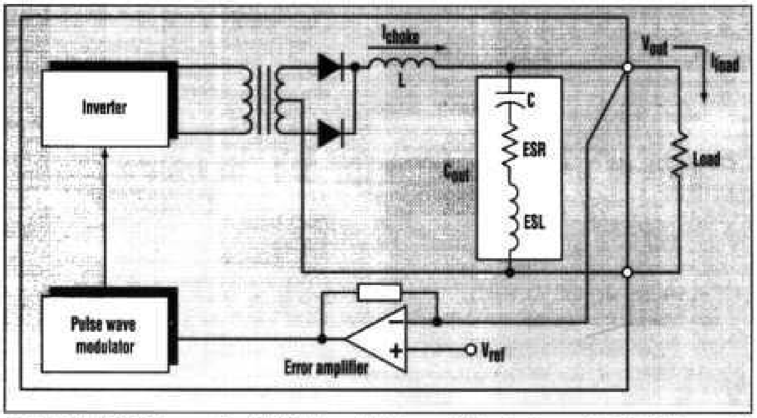
Understanding the mechanism of response to transients of switch-mode power supplies is essential for the proper selection and use of these supplies. Transient analysis is often based on the so-called "small-signal model" that assumes transient deviations in the closed feedback loop are so small that all loop components remain within their linear region. Unfortunately, in many applications, a load change may be large and rapid enough to drive the error amplifier into saturation such that small-signal analysis becomes invalid.

Further complicating the issue is the fact that the error amplifier often takes its input from the terminals of the supply. As a result, voltage drops along the load cables due to large, fast-changing load currents may not be accurately compensated for. While computer simulation or differential equations may be used here to predict circuit behavior, large-signal models are rarely available for the power-supply user. However, some rough estimates of voltage deviations can help users in this situation find a suitable compensating capacitor.

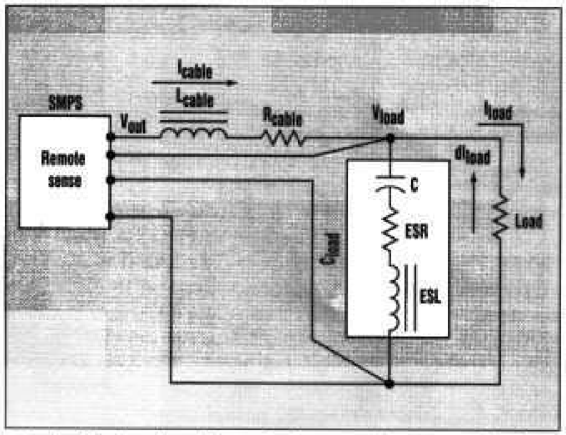
In a simplified circuit of a switch-mode power supply (SMPS), an error amplifier (EA) compares output voltage V_{out} with a reference V_{ref} and controls the duty cycle, D, via a pulse-width modulator (PWM) *(Fig. 1)*. The output capacitor C_{out} is represented by its equivalent circuit that includes the equivalent series resistance (ESR) and the equivalent series inductance (ESL). When we have a load step ΔI (we will assume ΔI is positive, that is the load increases), current through choke L cannot be instantly changed. No matter how quick the control circuit is, there is a finite time t needed for L to accommodate ΔI:

$$t > \frac{L\Delta I}{(V_{in}D_{max}) - V_{out} - V_{diode}}$$

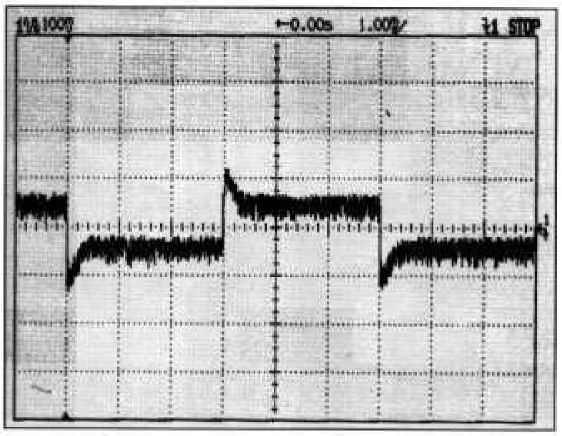
where D_{max} = the maximum duty cycle



1. This simplified diagram of an SMPS shows that the switching load current in the first moment flows through the output capacitor, represented by an equivalent series resistance (ESR) and an equivalent series inductance (ESL). The ESR and ESL cause the output-voltage deviation.



2. Load cables introduce their own inductance and resistance. Therefore the peak transient deviation and response times specified in the product data books are normally only valid when measured right at the power-supply's terminals, unless otherwise specified.



3. Output-voltage deviation with continuous load transients between 25 A and 50 A (50-µs transition time) measured at the output connector. Slightly different levels of steady-state voltage at different I_{load} allow current sharing and redundant operation.

and V_{diode} = the diode's voltage drop.

Until I_{choke} slews to the new load current, the switching component of I_{load} flows through C_{out}. This results in an output-voltage deviation ΔV_{out} that may be as much as:

$$\Delta V_{out(max)} \leq \frac{ESL(dI_{load})}{dt} + ESR(\Delta I)$$

where dI_{load}/dt is the load-current's slew rate (amps per second). While the SMPS's output capacitors act as a reservoir for these transient currents, the number of capacitors used is normally a trade-off for the manufacturer between cost, size, and transient response.

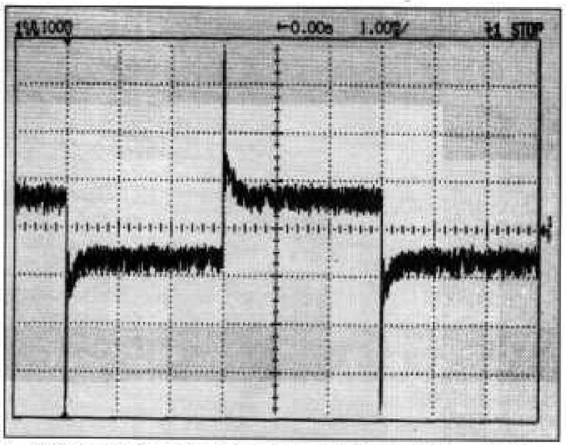
Cable Effects

The delay in the supply's inductor is only half the problem. When load cables are introduced, all the ground rules change. An SMPS product catalogs often specify two values: peak transient deviation and response time. But because load cables always have a certain self-inductance, L_{cable}, and a resistance, R_{cable}, these data are normally valid only when measured right at the power-supply terminals, unless otherwise noted *(Fig. 2)*. When I_{load} changes, Faraday's law tells us L_{cable} will cause an initial voltage deviation ΔV of:

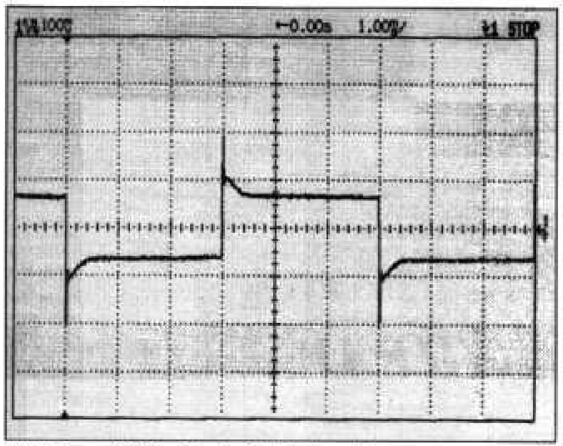
$$\Delta V = \frac{-L_{cable}(dI_{load})}{dt}$$

In addition, R_{cable} will cause an output voltage drop as I_{load} slews.

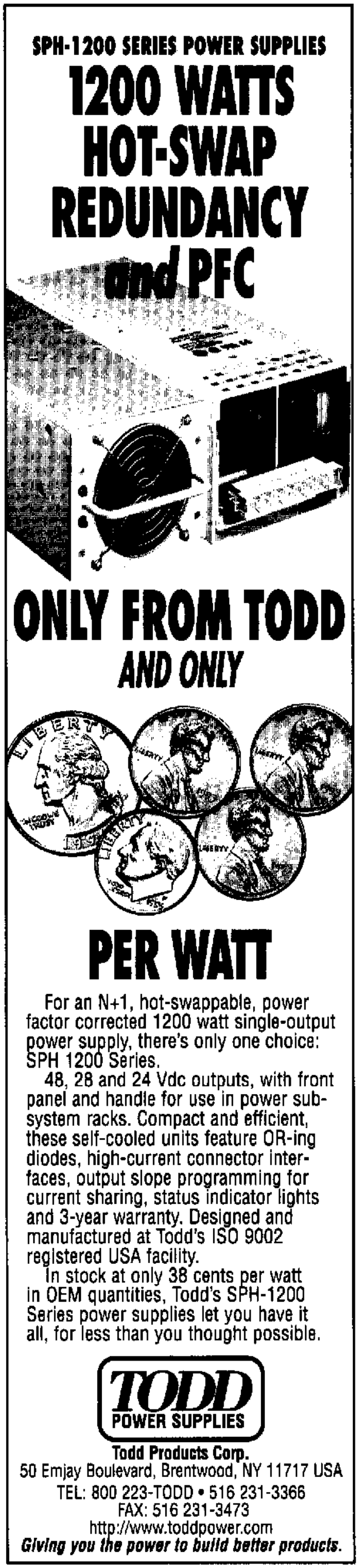
As an example, the typical inductance of AWG#10 stranded hook-up wire is 0.15 µH/foot. For a 1-ft. pair, we will have an inductive glitch of 150 mV for the load step of 0.5 A/µs, a glitch of 300 mV for 1 A/µs, and a whopping inductive glitch of 3 V for 10 A/µs. This initial deviation does not depend on the power supply, as it is purely a function



4. Again, the continuous load transients are between 25 A and 50 A, but the load is connected via a pair of 1-ft. cables (AWG#10) with a 0.1-µF terminating capacitor. The larger peak transient deviation is due to the inductance of the load cables.



5. This time, a 3900-µF terminating load capacitor serves as a reservoir for the 25- to 50-A transient current. The capacitor's low ESL and high capacitance reduce peak transient deviation as well as ripple to give a smoother ouput waveform.



of the load cables and the load's dI_{load}/dt. The only thing that may effectively reduce ΔV is an external load capacitance.

While computer simulation or differential equations may be used to find the exact transient response (and thus find a suitable compensating capacitor), the problem is that we need accurate large-signal models of an SMPS power stage, PWM, and error amplifier. Since this "inside" information is rarely available to a power-supply user, we will try to provide some rough estimates that could help the SMPS user that is attempting transient analysis.

The time needed to change a current through load cables is given as:

$$t_1 \cong t_{delay} + t_{rise} \qquad \text{eq.1}$$

where t_{delay} = the SMPS delay time and t_{Rise} = the time needed for I_{cable} to catch up to the load current. This rise time is given as:

$$t_{rise} = t_{delay}\left(\frac{\dfrac{dI_{load}}{dt}}{\left(\dfrac{V_{max} - V_{load}}{L_{cable}}\right) - \dfrac{dI_{load}}{dt}}\right)$$

where V_{max} is the maximum output voltage during the transient recovery of the supply.

During this time, the load current will slew up to $t_1 dI_{load}/dt$, and it can be shown that this may cause the output voltage to dip by as much as:

$$\Delta V_{out(max)} < ESR\left(\frac{t_1 dI_{load}}{dt}\right) + t_1^2\left(\frac{dI_{load}/dt}{C_{load}}\right) \qquad \text{eq.2}$$

A Typical Scenario

For example, an SMPS has a nominal V_{out} of 5 V and V_{max} = 5.5 V. The load changes from 25 A to 50 A (ΔI =25 A) over a 50-µs time span (dI_{load}/dt=0.5 A/µs); t_{delay} is 20 µs and the inductance of the load cable is 0.3 µH (which is the inductance of a pair of stranded wires AWG#10 measuring 1 ft. each). Suppose the load cables are terminated with a capacitor rated at 3900 µF, 10 V (LXF series, United Chemi-Con), and with an ESR of less than 24 mΩ.

As shown in equation 3, the time needed for I_{cable} to catch up with I_{load} would be t_1 = 29 µs. Judging from equation 4, $\Delta V_{out(max)}$ is less than 0.45 V. If this deviation is not acceptable, another capacitor has to be connected parallel to the load.

The effects of load cables and external capacitors on the example of transient response of a Todd TMX-350 prototype for a continuous load transient between 25 A and 50 A, with a transition time of 50 µs (0.5 A/µs), are shown *(Figs. 3, 4, and 5)*. The output-voltage deviation when the load is connected directly to the output connector is shown *(Fig. 3, again)*. The slightly different levels of steady-state voltages at different load currents (droop) allow automatic current sharing of two or more power supplies and provide glitch free "hot swaps." These output-level changes are typically around 2%.

The response (with remote sense) when the same load connected via a pair of AWG #10-size stranded wires measuring 1 ft. each, with a 0.1-µF ceramic capacitor and no external electrolytic capacitors, also is shown *(Fig. 4, again)*. The response of the same circuit, with a 3900-µF, 10-V United Chemi-Con, LXF series terminating load capacitor is much improved *(Fig. 5, again)*.

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HOW VALUABLE	**CIRCLE**
HIGHLY	532
MODERATELY	533
SLIGHTLY	534